

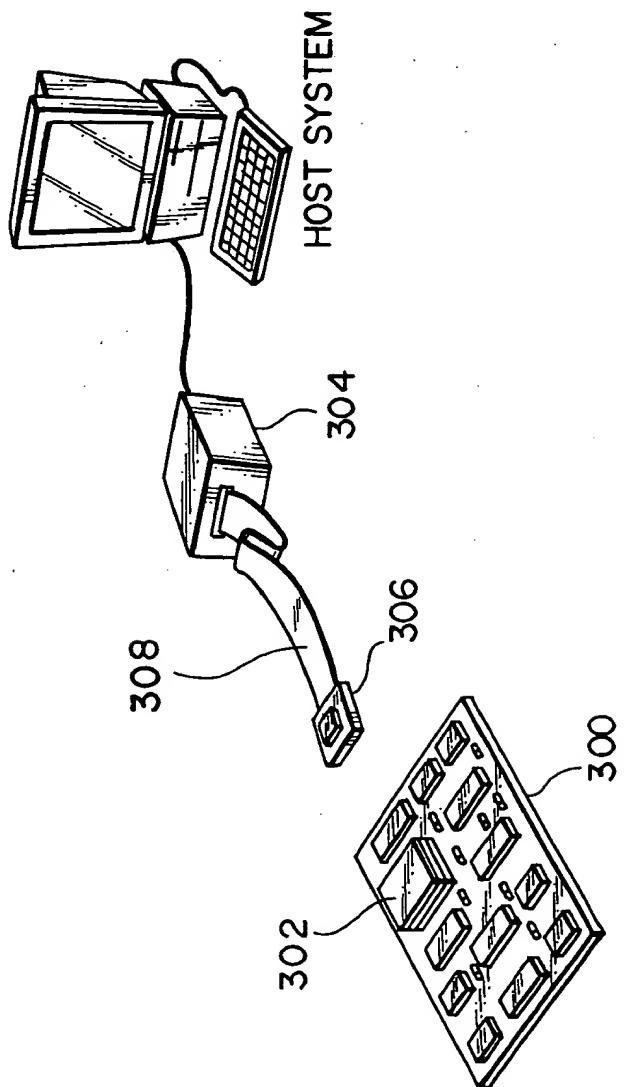
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FIG. 1



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FIG. 2A

USER MODE

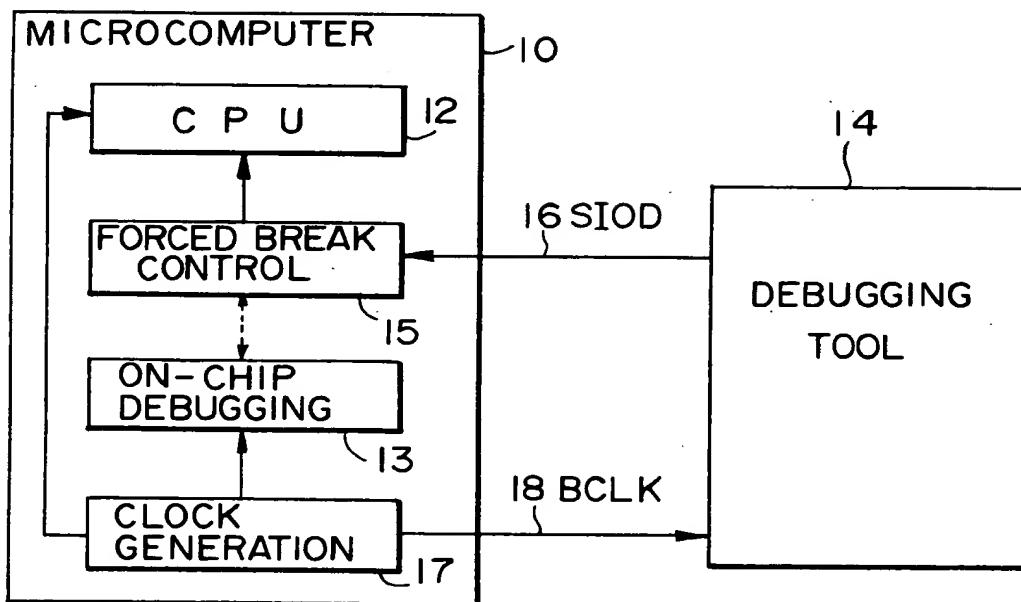


FIG. 2B

DEBUGGING MODE

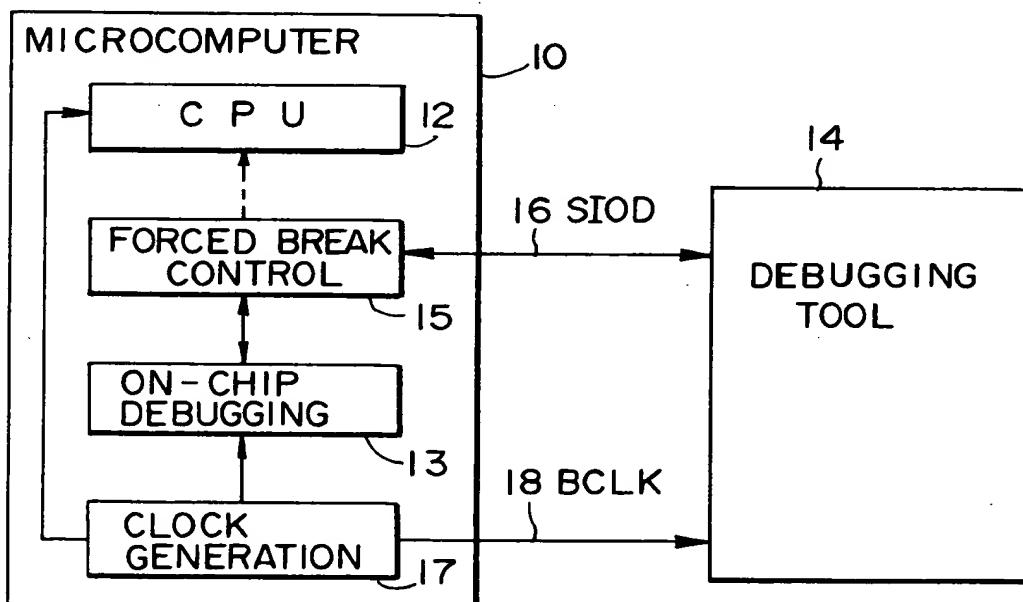
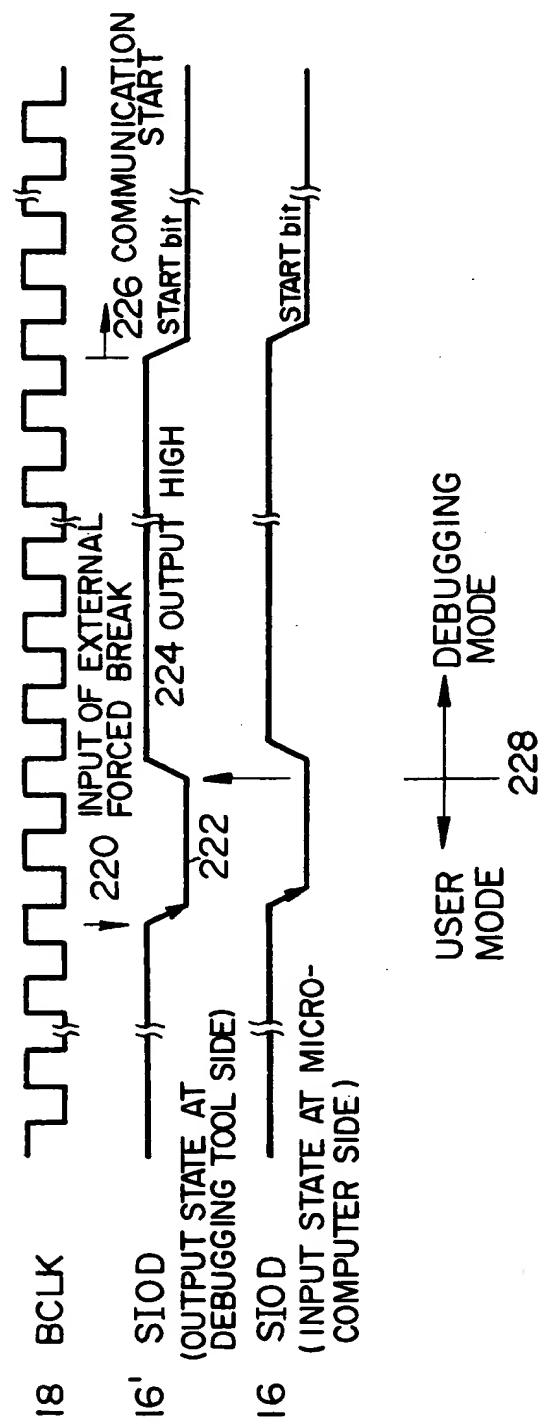


FIG. 3



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FIG. 4A

WHEN NO DEBUGGING TOOL IS CONNECTED

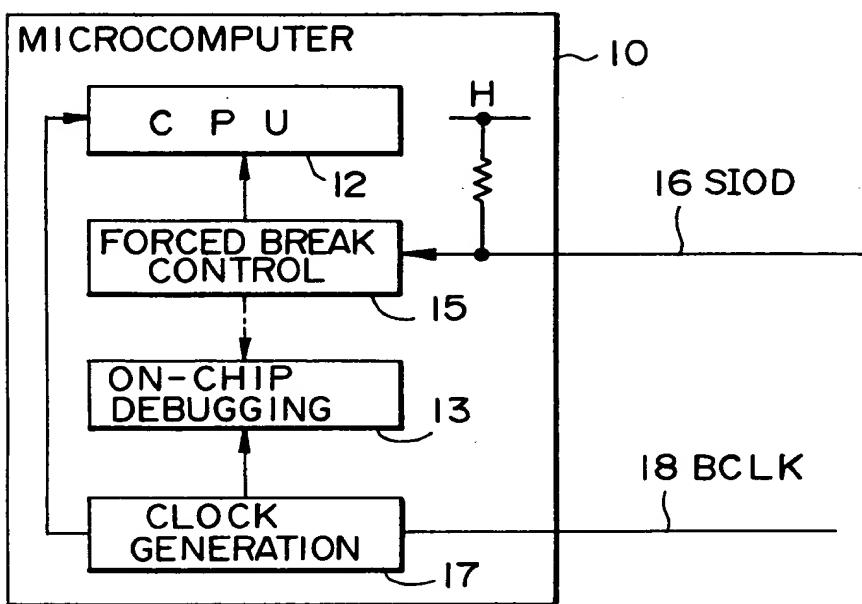
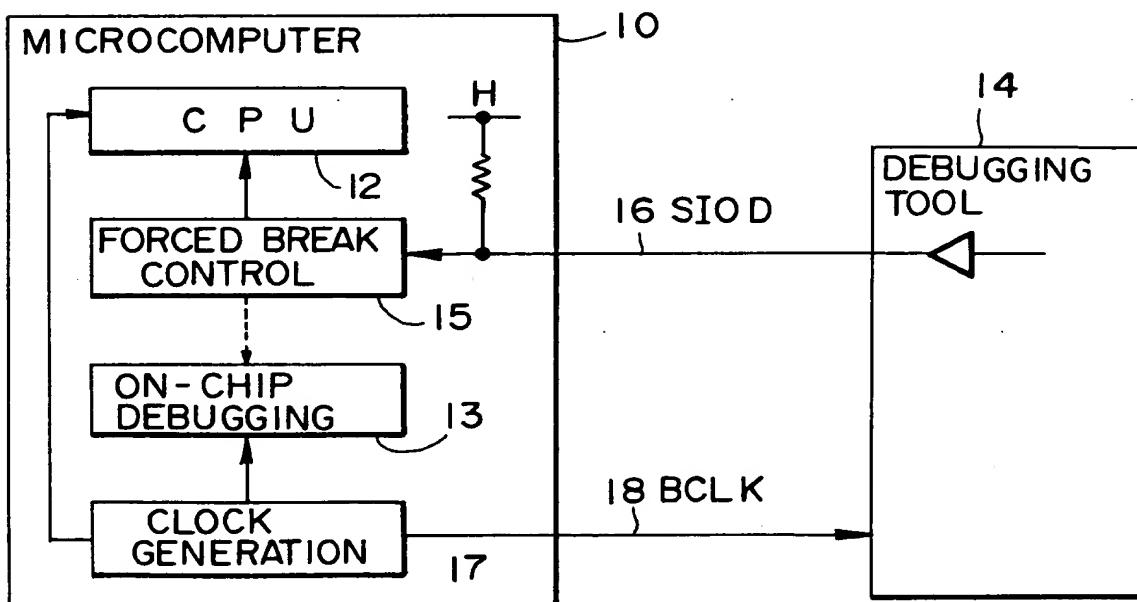


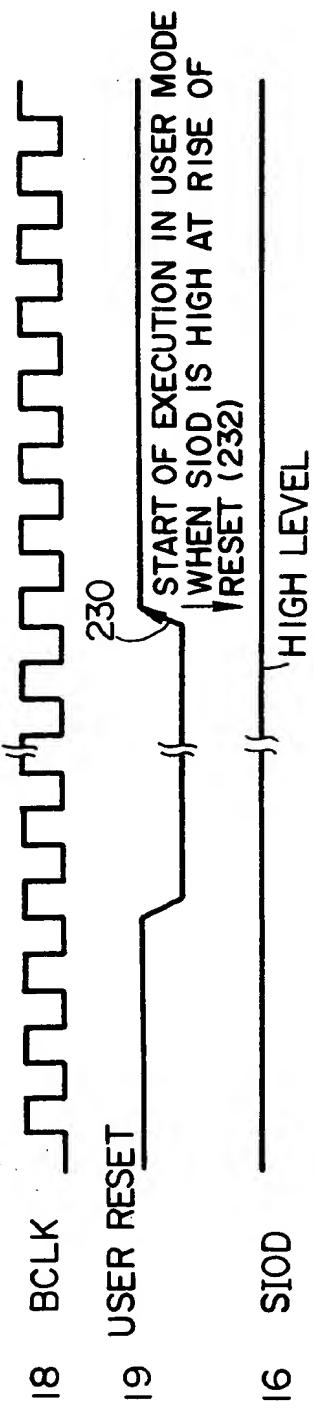
FIG. 4B

WHEN DEBUGGING TOOL IS CONNECTED

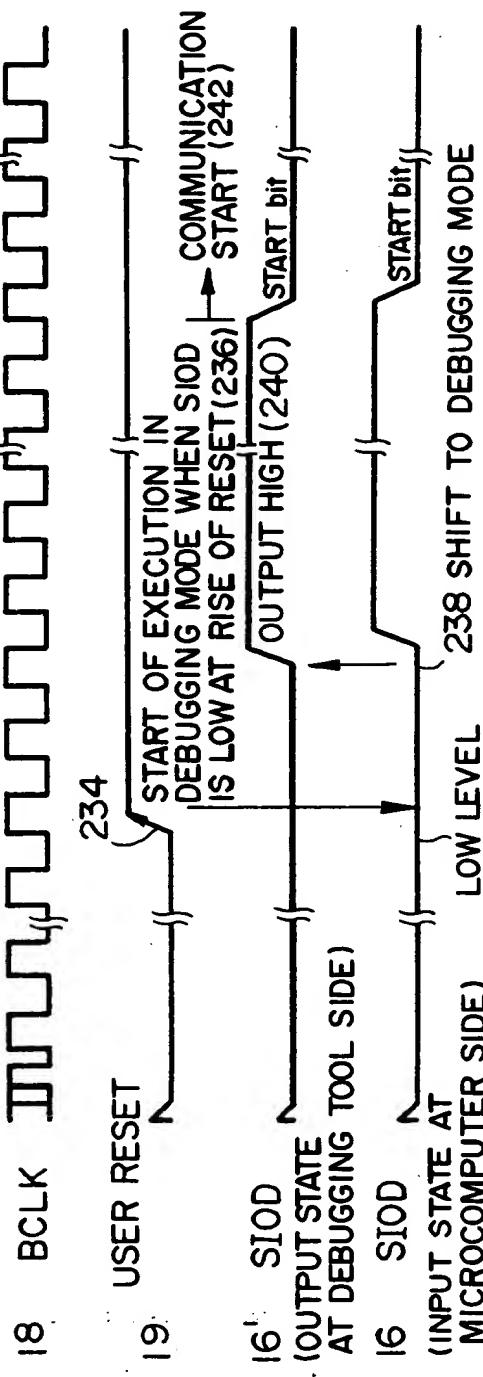


*FIG. 5A*

WHEN NO DEBUGGING TOOL IS CONNECTED

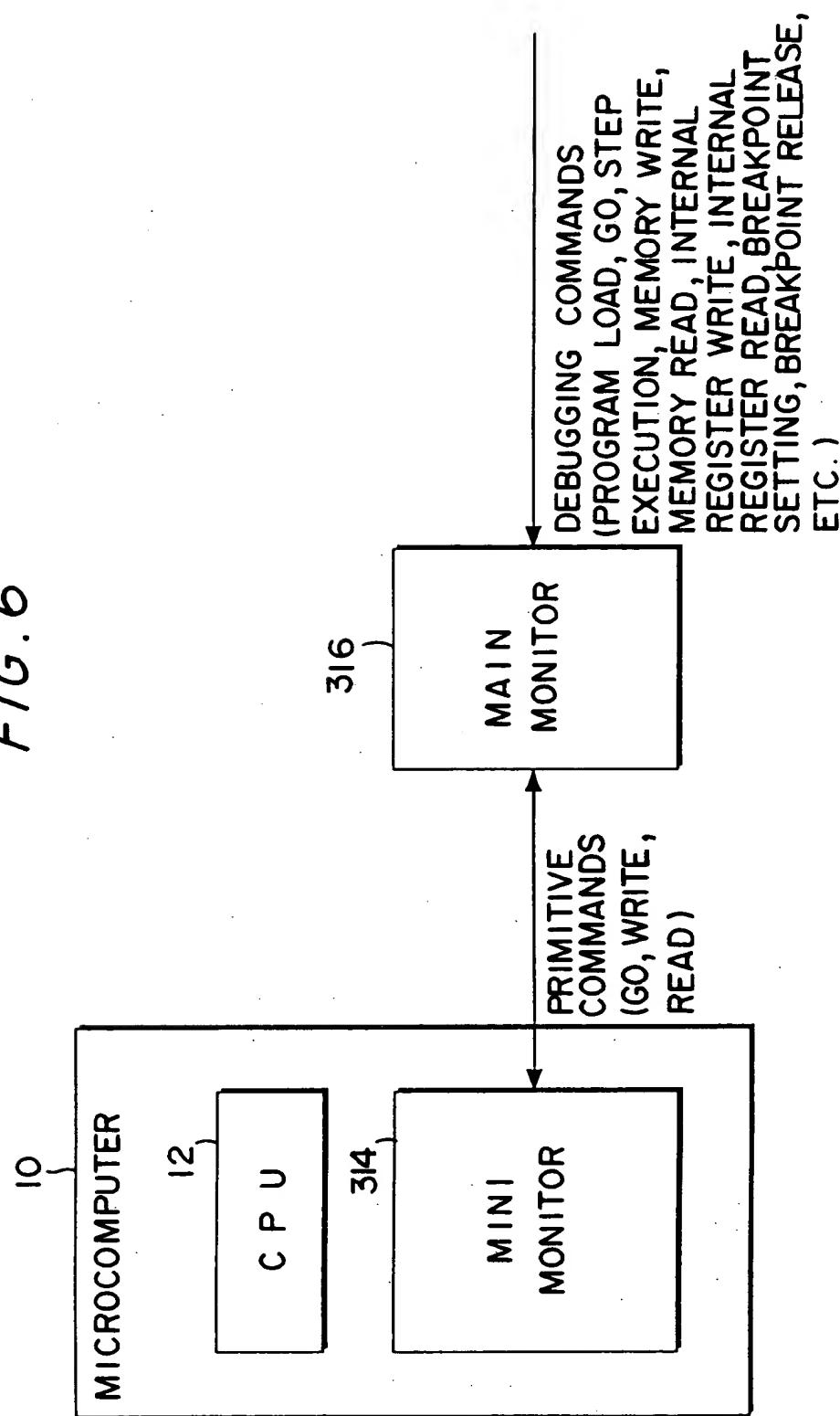
*FIG. 5B*

WHEN DEBUGGING TOOL IS CONNECTED



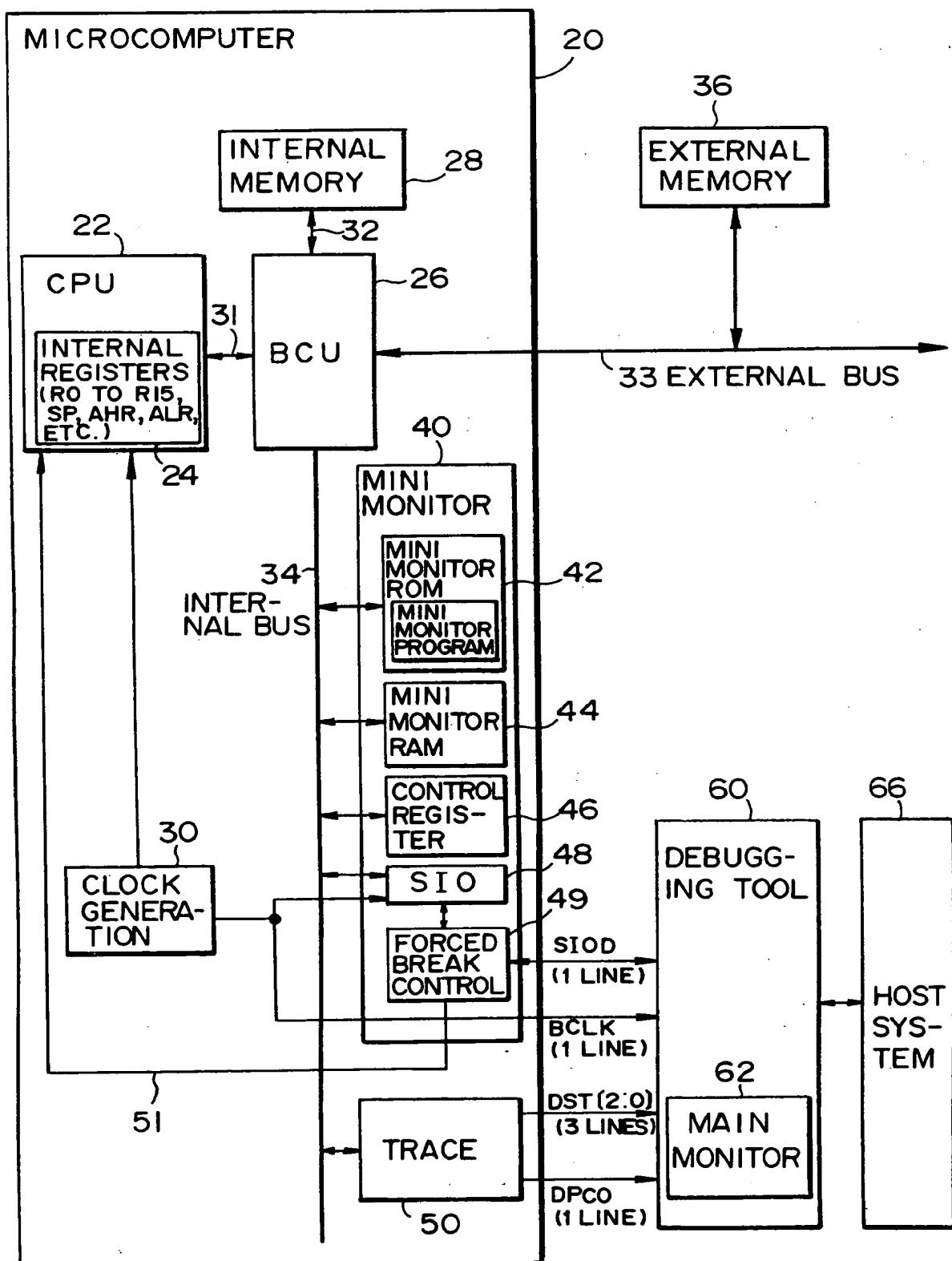
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FIG. 6



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FIG. 7

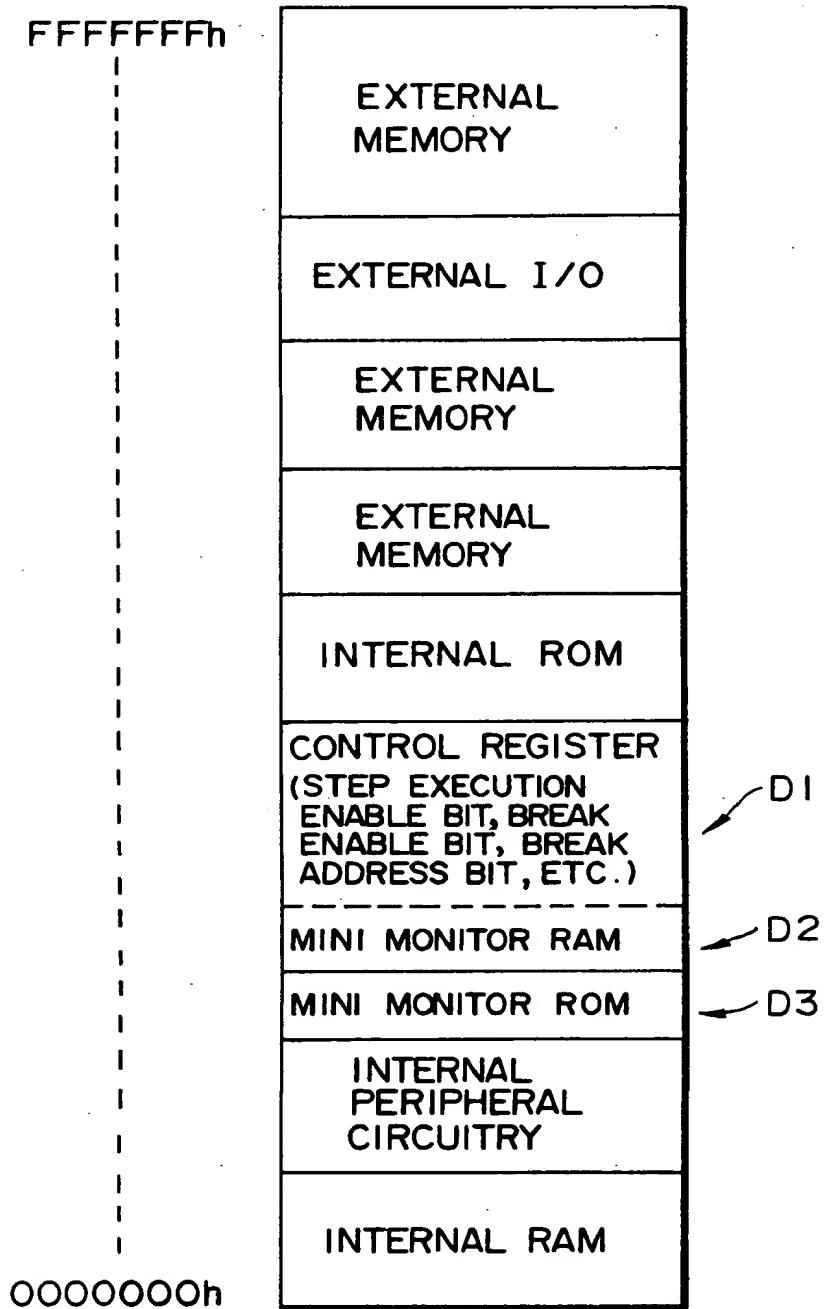


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FIG. 8

## MEMORY MAP IN DEBUGGING MODE

FFFFFFFFFFh



0000000h

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FIG. 9A

PROGRAM LOAD

$\left( \begin{matrix} 80010h, 12 \text{ BYTES}, \text{ADD} \dots, \text{SUB} \dots \\ (\text{AND} \dots, \text{OR} \dots, \text{XOR} \dots, \text{LD.W} \dots) \end{matrix} \right)$

WRITE(80010h, ADD..., SUB --- )  
+ WRITE(80014h, ADD..., OR --- )  
+ WRITE(80018h, XOR..., LD.W --- )

FIG. 9B

STEP EXECUTION

WRITE TO STEP EXECUTION ENABLE  
BIT OF CONTROL REGISTER  
+ GO

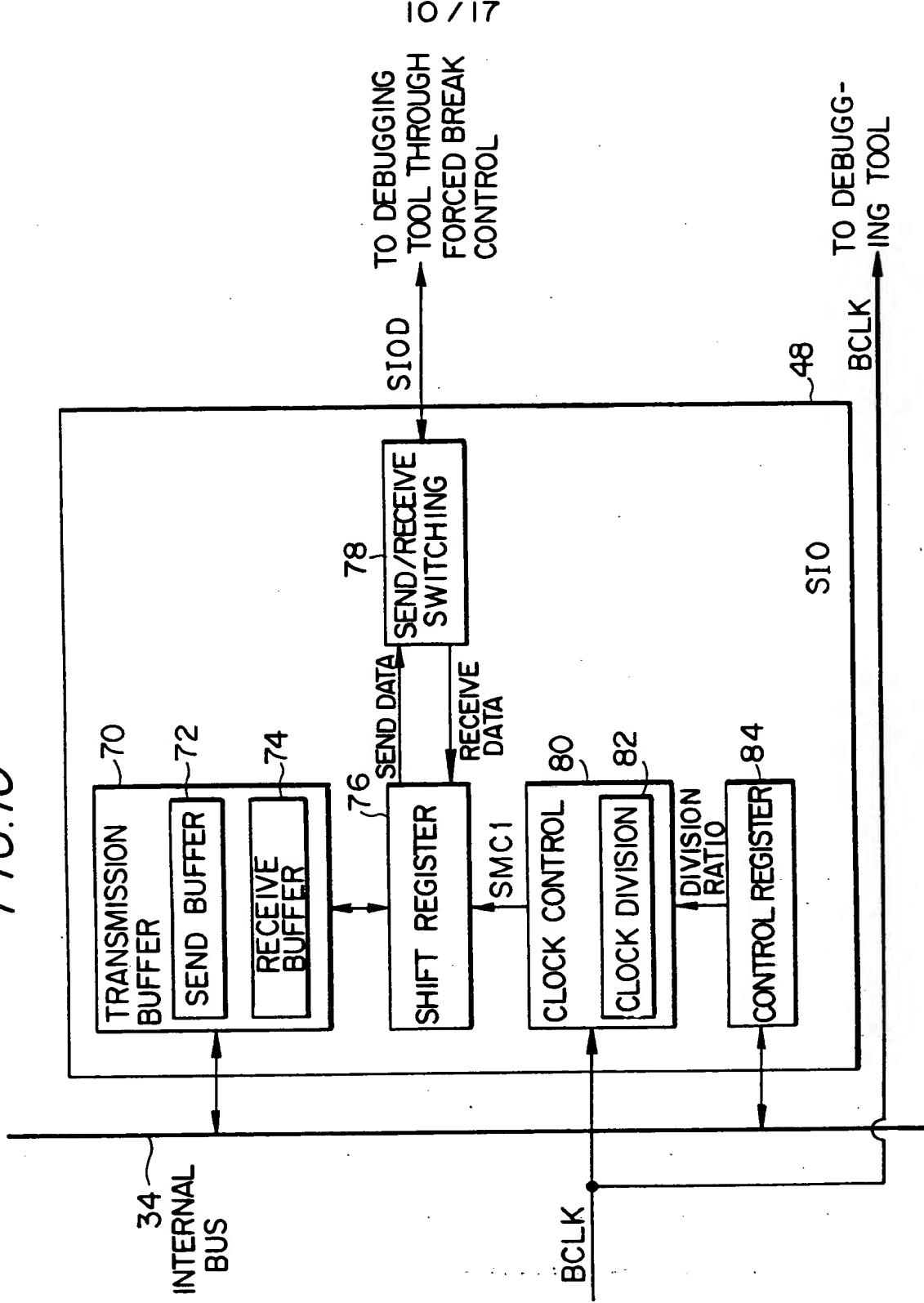
FIG. 9C

INTERNAL REGISTER READ  $\rightarrow$  READ OF MONITOR RAM ON MEMORY MAP

FIG. 9D

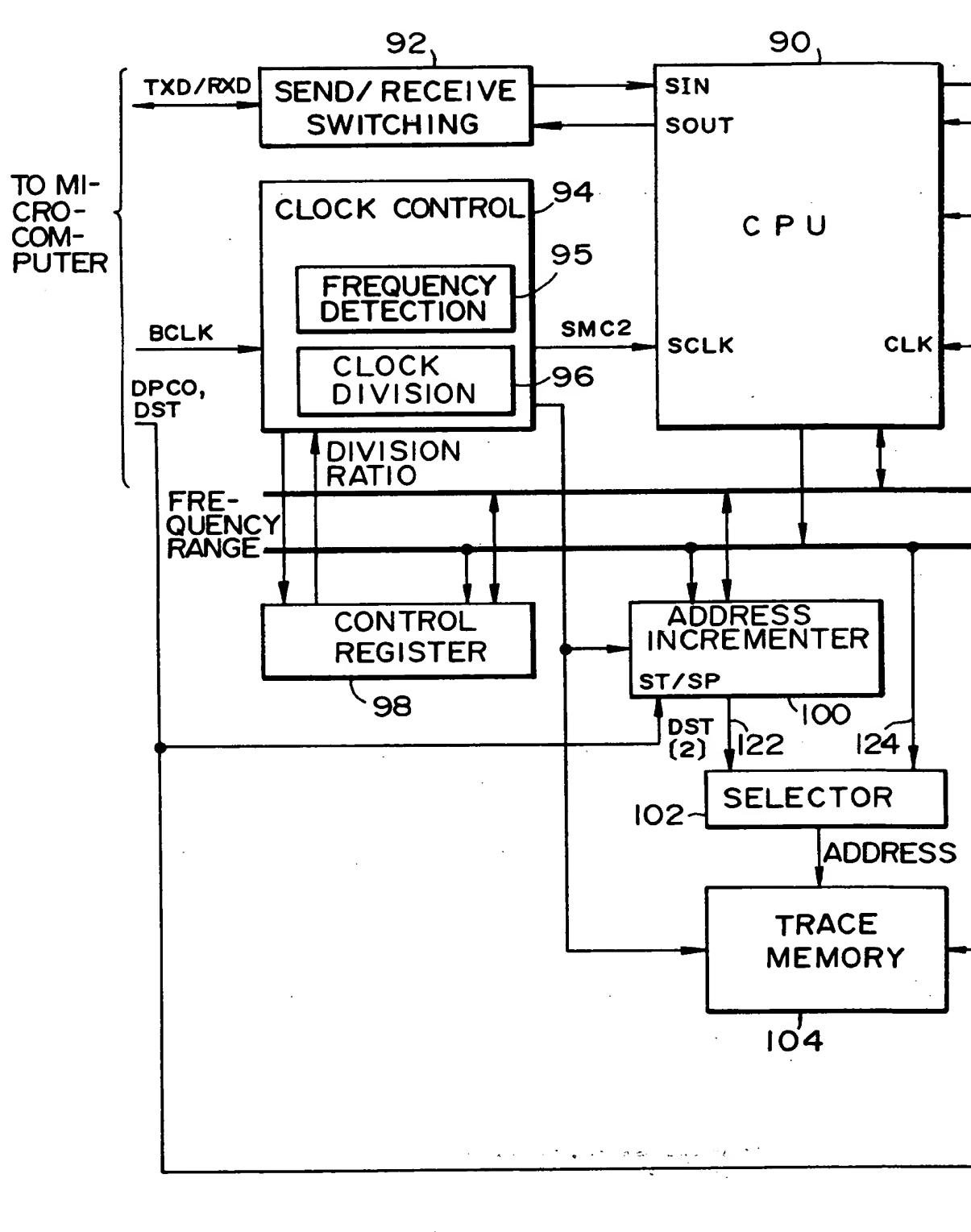
BREAKPOINT SETTING  $\rightarrow$  WRITE TO BREAK ENABLE BIT AND  
BREAK ADDRESS BIT OF CONTROL  
REGISTER

FIG. 10



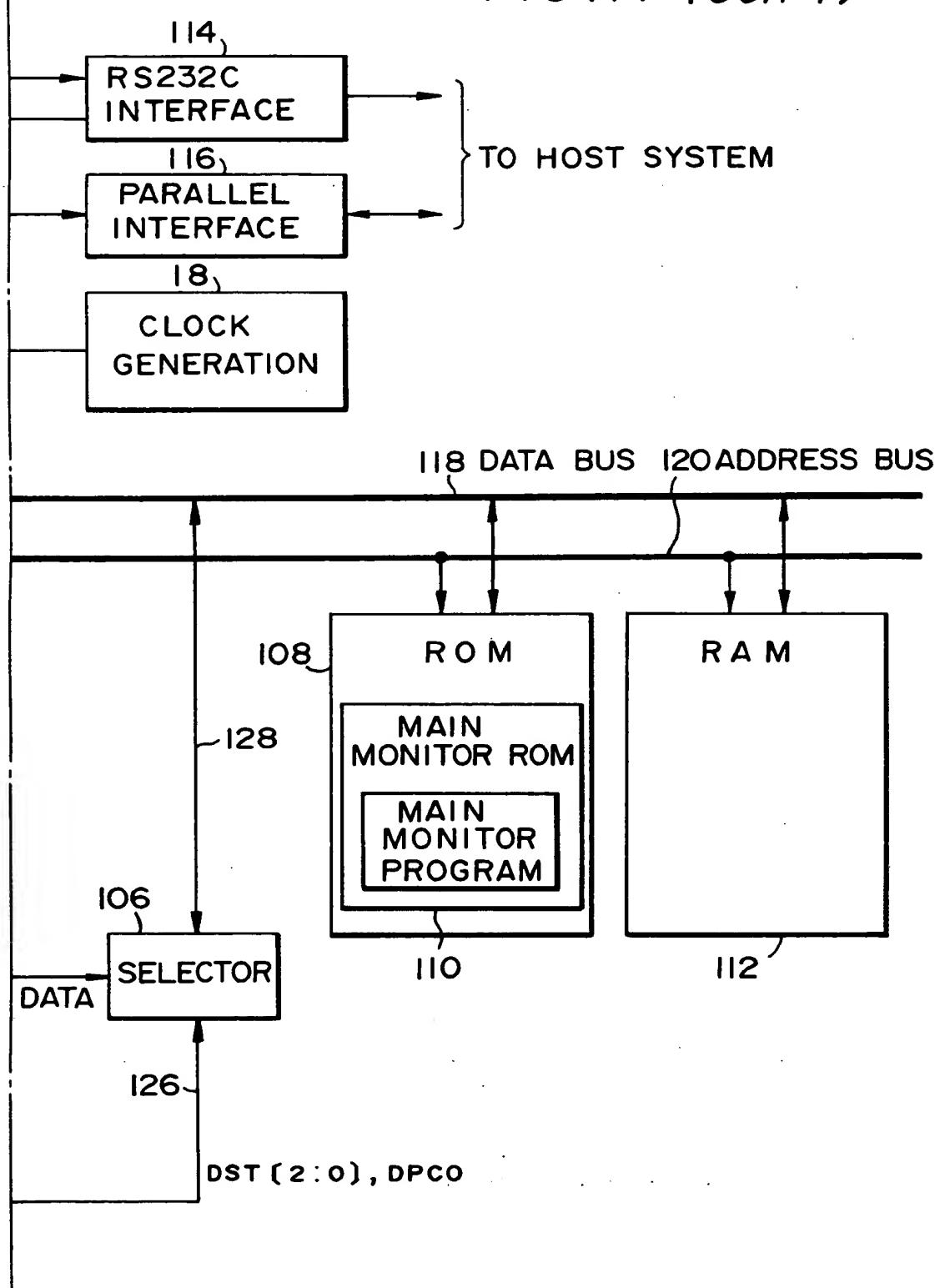
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FIG. 11



11/17 (con't)

FIG. 11 (con't)



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FIG. 12A

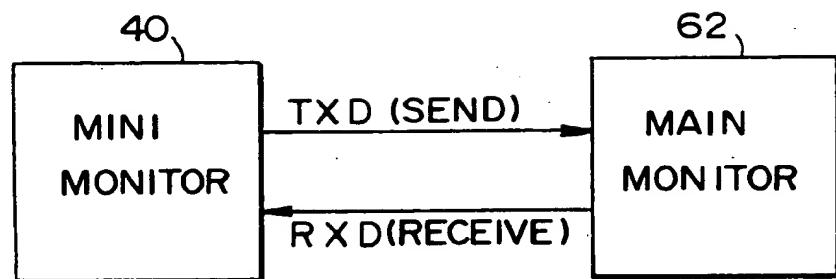


FIG. 12B

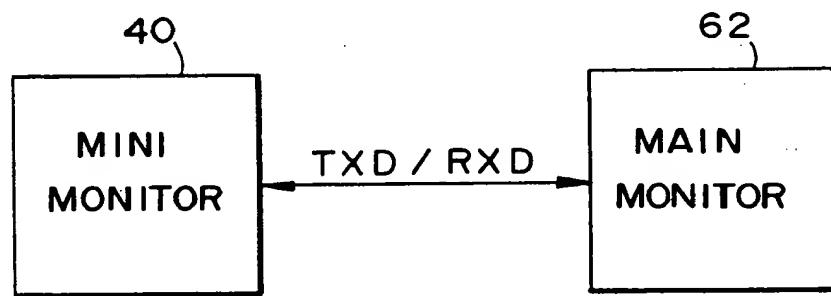
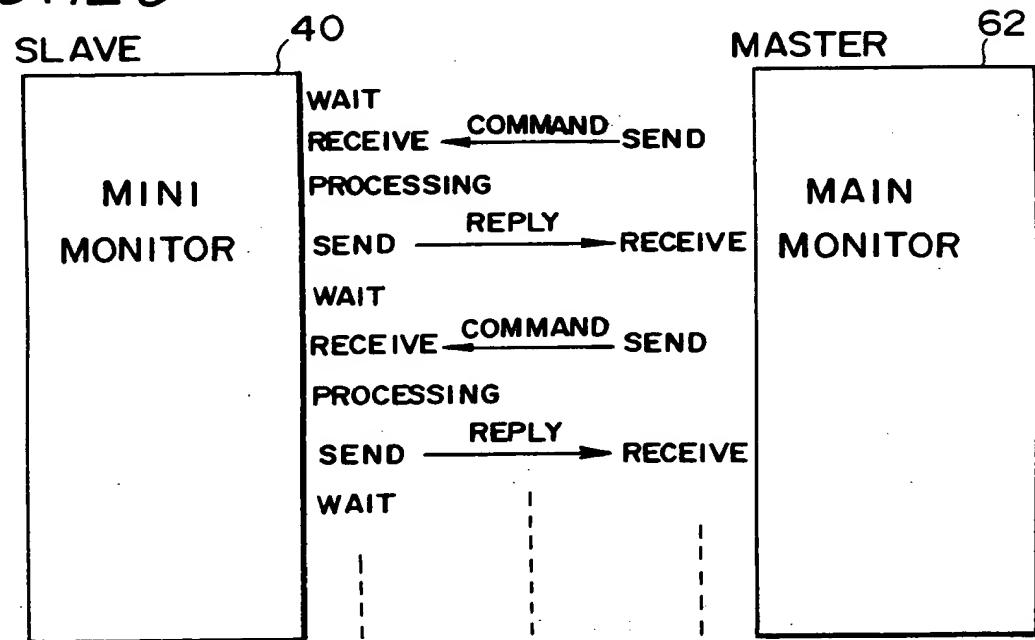
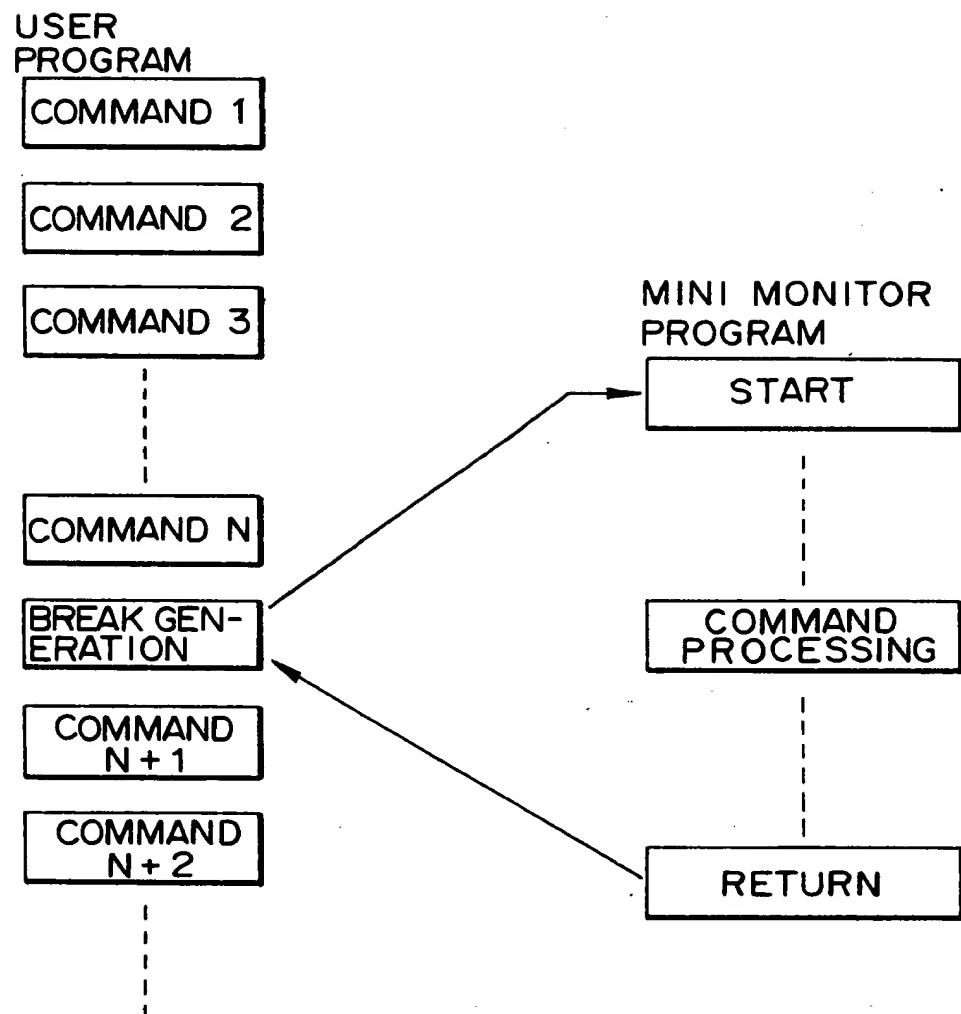


FIG. 12C



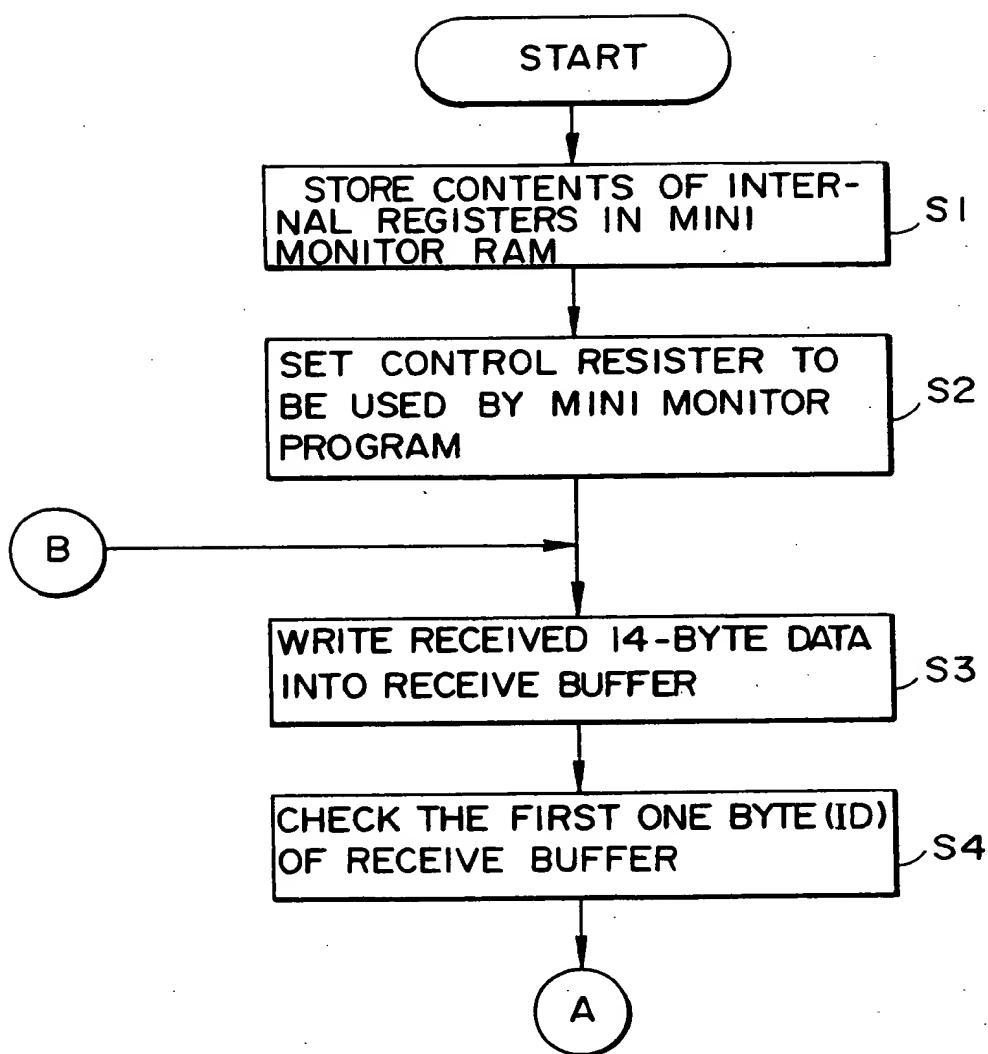
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FIG. 13



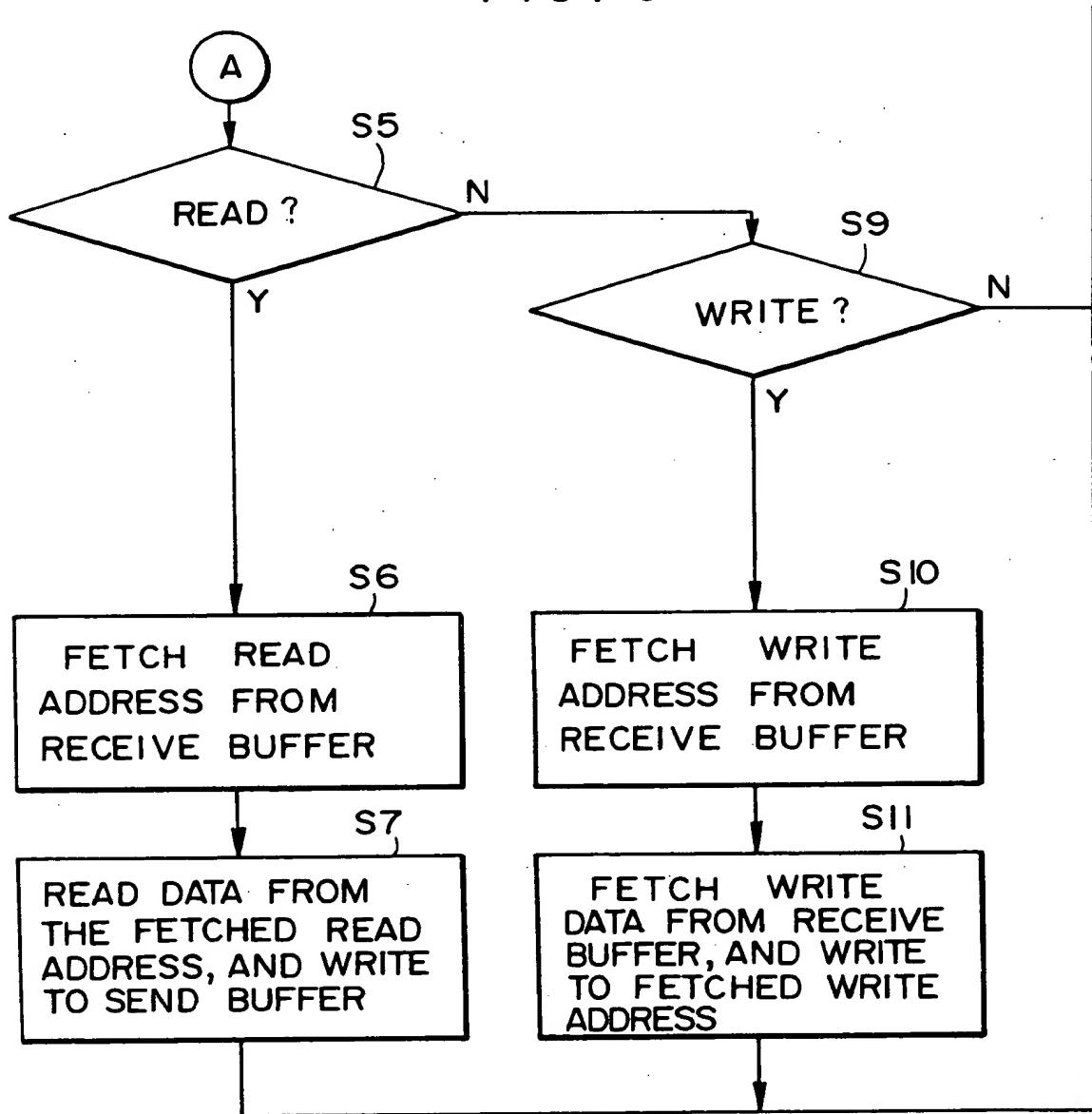
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FIG. 14



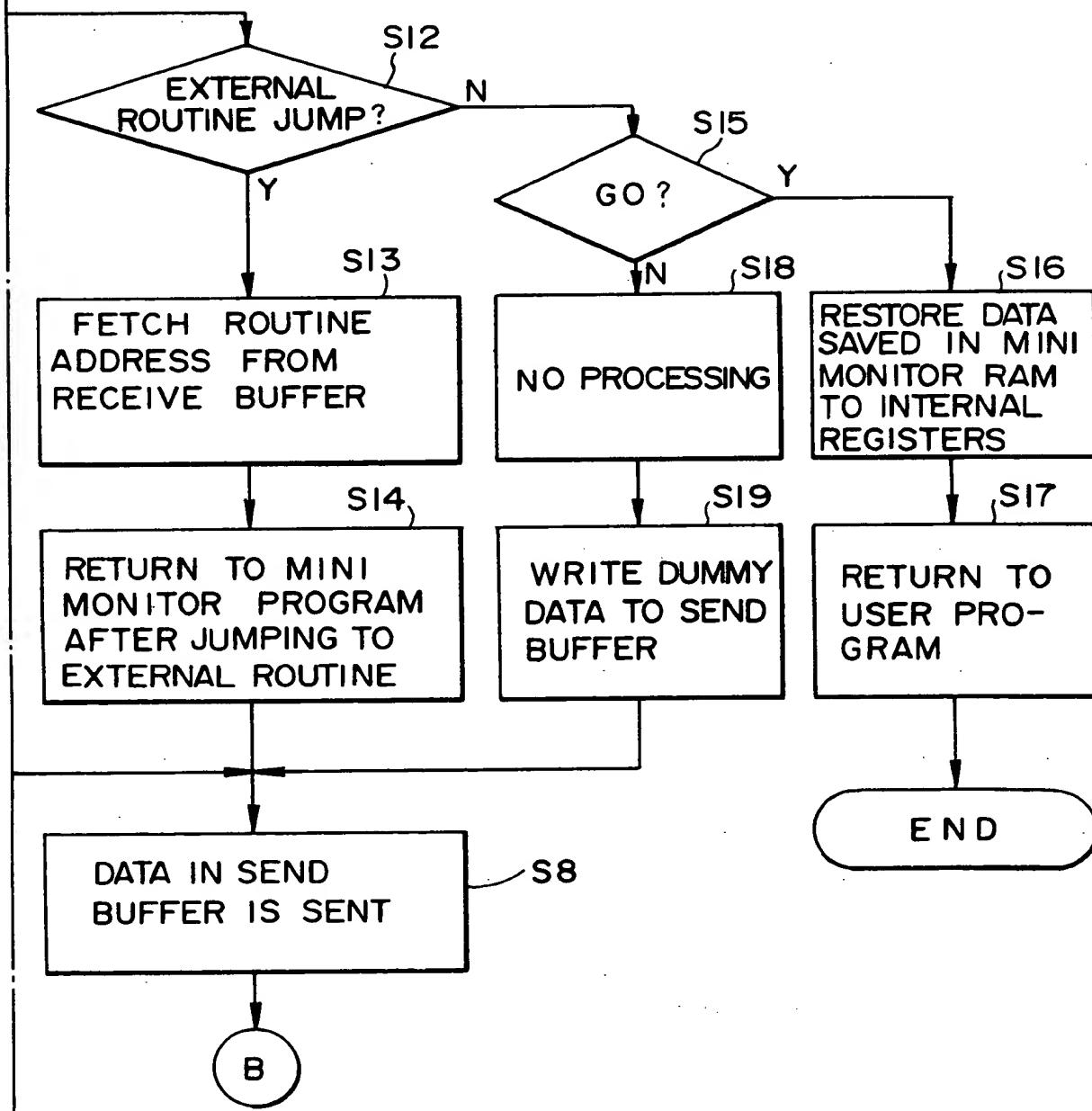
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FIG. 15



15 / 17 (con't)

FIG. 15 (con't)



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FIG. 16A

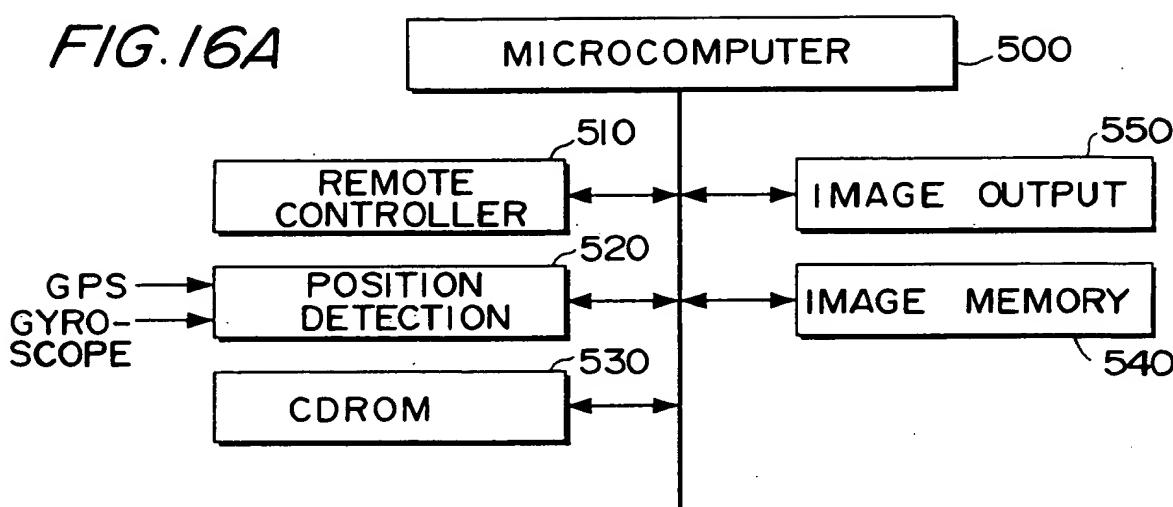


FIG. 16B

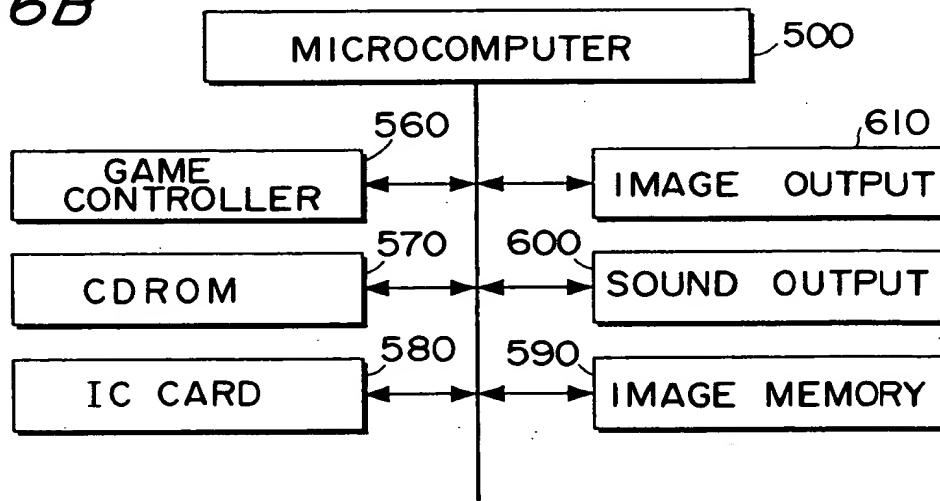
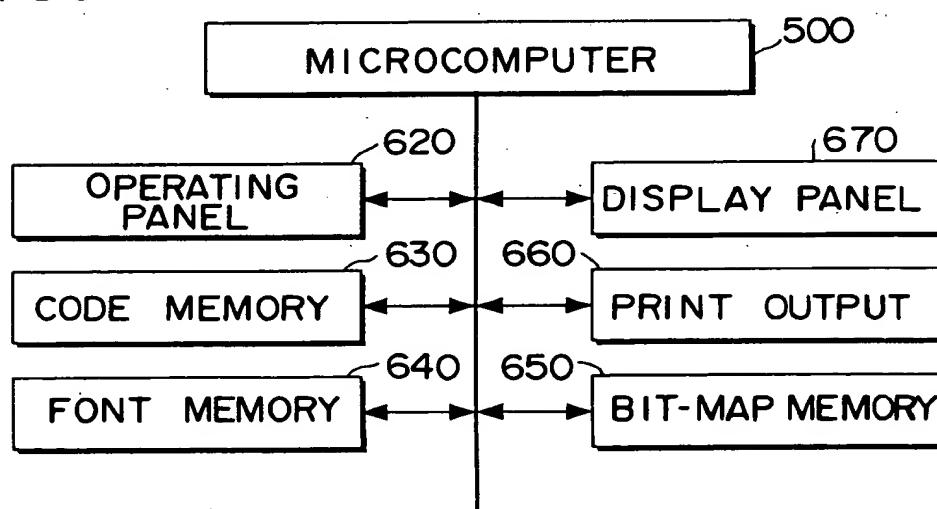
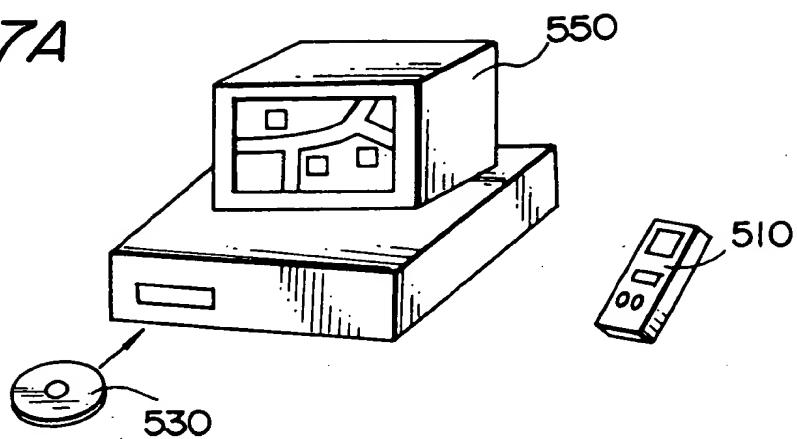
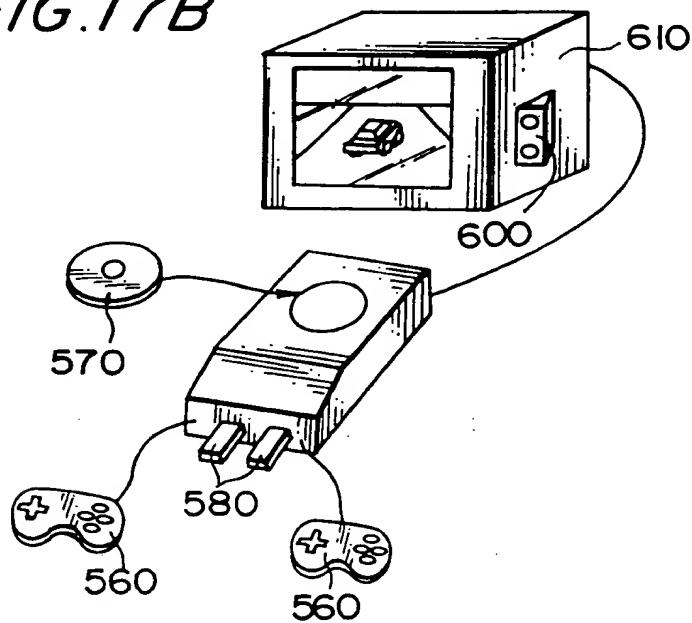


FIG. 16C



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*FIG.17A**FIG.17B**FIG.17C*